International Journal of Scientific & Engineering Research, Volume 4, Issue 5, May-2013
ISSN 2229-5518

A novel dead time elimination method for single phase four level voltage source inverter

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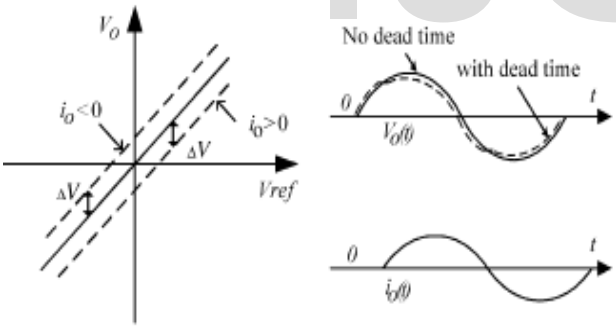
Abstract- Dead time is a short delay introduced between the gating signals of the upper and lower switches in an inverter leg to prevent the short circuit of dc link. Such dead time results in a change in f undamental voltage and also causes low frequency distortion. In this paper , a novel method for the elimination of dead time in four level voltage source inverter is proposed and implemented. This method reduces the low frequency distortion and results in a steady fundamental voltage.. The performance has been analyzed by the PSPICE Simulation. The output shows better performance results.

Index terms – Dead-time, harmonic, phase-leg, gate drive, voltage source inverter (VSI)

1 INTRODUCTION

To avoid shoot-though in PWM controlled voltage source inverters (VSI), dead-time, a small interval during which both the upper and lower switches in a phase leg are off, is introduced into the control of the standard VSI phase leg.However, such a blanking time can cause problems such as output waveform distortion and fundamental voltage loss in VSIs.[1-4]Fig.1 shows the dead-time effect in a voltage source inverter. Fig 1 (b) shows the output voltage waveform distortion caused by dead-time effect.



(a) **(b)**

Fig.1.Dead time effect

To overcome dead-time effects, most solutions focus on dead-time compensation [1-4] by introducing complicated PWM controller and expensive current detection hardware. In practice, the dead-time varies with the devices and output current, as well as temperature, which makes the compensation less effective, especially at low output current, low frequency, and zero current crossing. [5] proposed a new switching strategy for PWM power converters. [6] presented an IGBT gate driver circuit to eliminate the dead-time effect. [7] proposed a phase leg configuration topology which prevented shoot through. However, an additional diode in series in the phase leg increases complexity and causes more loss in the inverter. Also, this phase leg configuration is not suitable for high power inverters because the upper device gate turn off voltage is reversely clamped by a diode turn on voltage. Such a low voltage, usually less than 2 V, is not enough to ensure that a device is in off state during the activation of its complement device.

In this paper , a novel method for the elimination of dead time in four level voltage source inverter is proposed and implemented. This method reduces the low frequency distortion and results in a steady fundamental voltage.. The performance has been analyzed by the MATLAB/Simulink. The output shows better performance results.

II PRINCIPLE OF DEAD-TIME ELIMINATION

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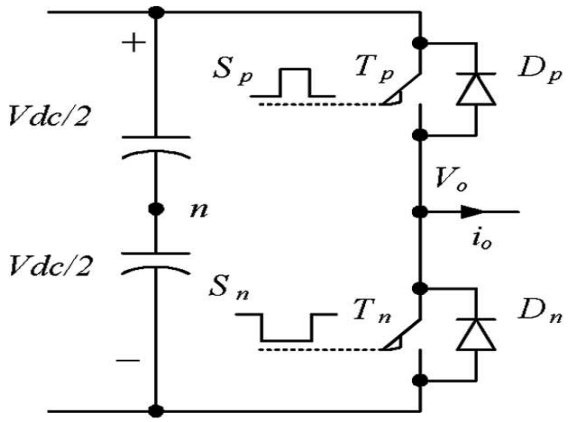


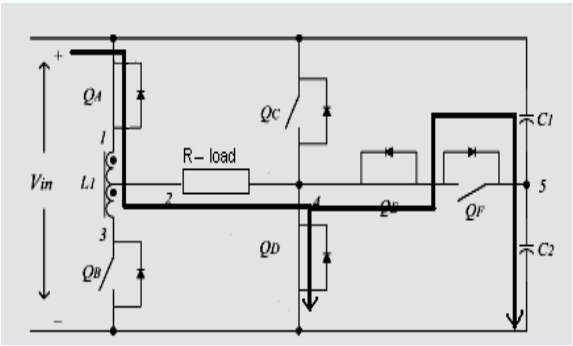
Fig. 2. A generic phase leg of VSIs.

To explain the principle of the proposed dead-time elimination method, we refer to a generic phase leg of VSIs, as shown in figure 2.

Assuming the output current flows out of the phase leg, in each switching cycle, the current comes out from the upper device when *Kp* is on and freewheels through diode *Dn* when *Kp* is off. Here this current direction is defined as positive. Under this condition, the generic phase leg can be equivalently expressed as a P type switching cell. Similarly when load current flows into the phase leg, defined as negative, the current goes into the lower device when *Kn* is on and freewheels through diode *Dp* when *Kn* is off. Under this condition, the generic phase leg can be equivalently expressed as a N type switching cell . Actually a generic phase leg is a combination of one P switch cell and one N switch cell. There is no question that dead-time is not required for either a P switch cell or a N switch cell because both cells are configured with a controllable switch in series with a uncontrollable diode.[8].

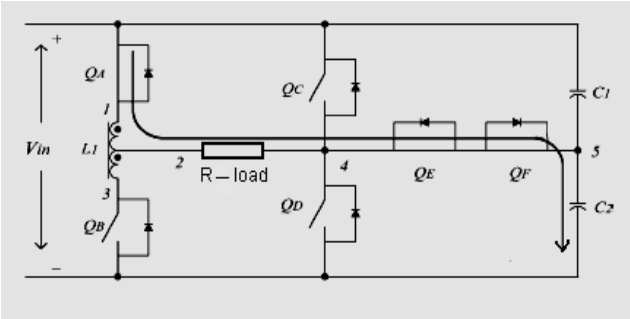
III MODES OF OPERATION

MODE 1 :(POSITIVE MODE)



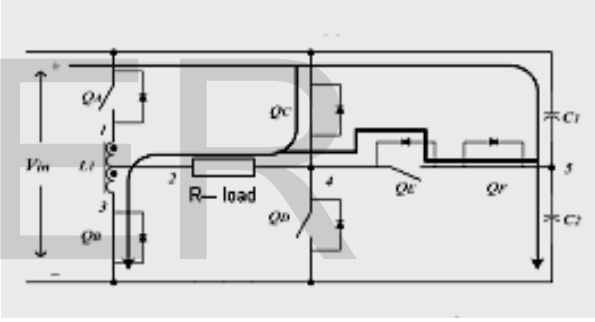
In this mode of operation the switches A and D of the full bridge and the switch E of the half bridge are in the conducting state and the corresponding current flow.

MODE 2 :(POSITIVE MODE)



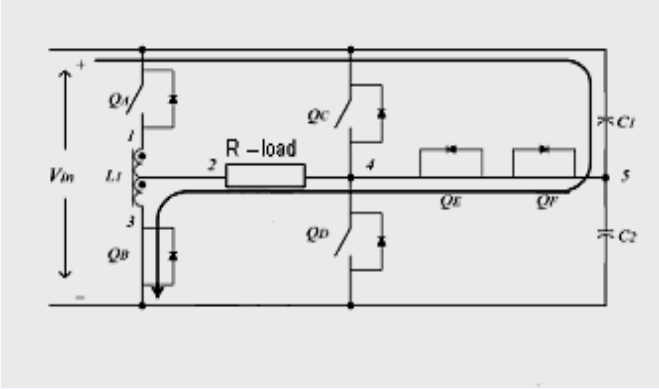
In this mode 2 operation switch A of the full bridge and the switches E and F of the half bridge are in the conduction state and the current flow in the circuit.

MODE 3(NEGATIVE MODE)



In this mode of operation the switches Band C of the full bridge, switch F of the half bridge are in the conduction state and the current flow in the circuit

MODE 4(NEGATIVE MODE)



In this mode of operation the switch B of the full bridge inverter circuit and the switches E and F of the half

bridge are in the conduction state and the current flow direction in the circuit.

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IV HARDWARE IMPLEMENTATION

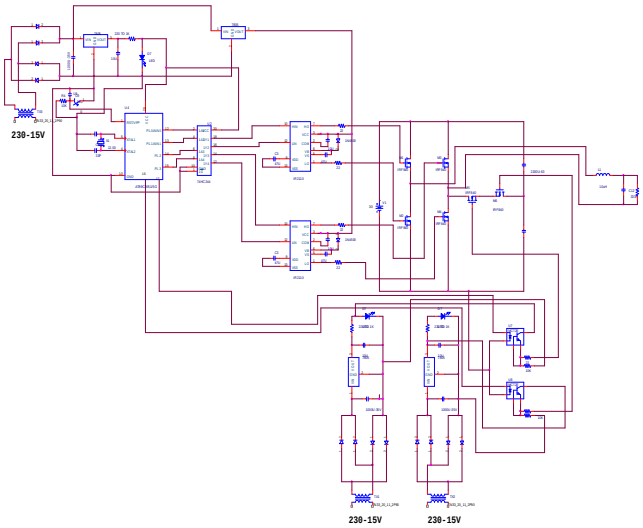

Fig.3.Hardware circuit diagram

The hardware circuit of the proposed method is shown in fig.3. The hardware circuit consists of the following major parts such as power supply unit, microcontroller circuit, buffer circuit and isolation circuit. Fig.4. and Fig.5. shows the main circuit and power and control circuit.

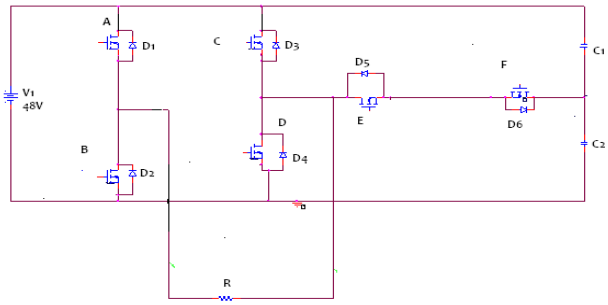

Fig.4.Main circuit

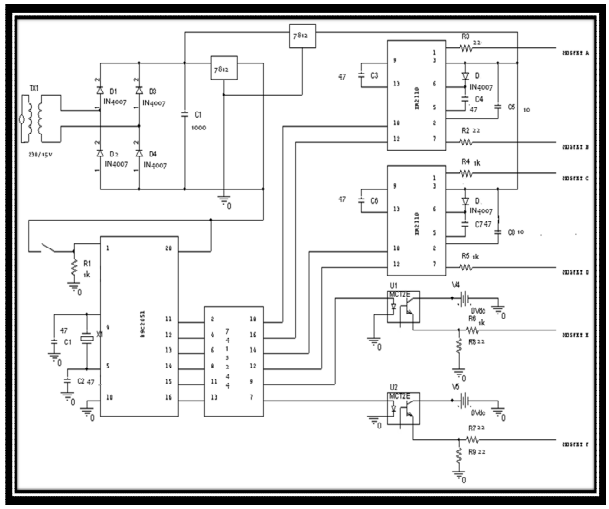

Fig.5.Power and control circuit

V SIMULATION RESULTS

In this paper, the simulation model is developed with PSPICE tool which contains a dc source, six MOSFETs , inductor, capacitor and a resistive load. The MOSFET is driven by the gate signal of frequency of 50KHZ. The circuit is designed for an output of 40V with an input of 48V. The simulation circuit of the proposed method and the output voltage waveform is shown in fig.6. and fig.7.

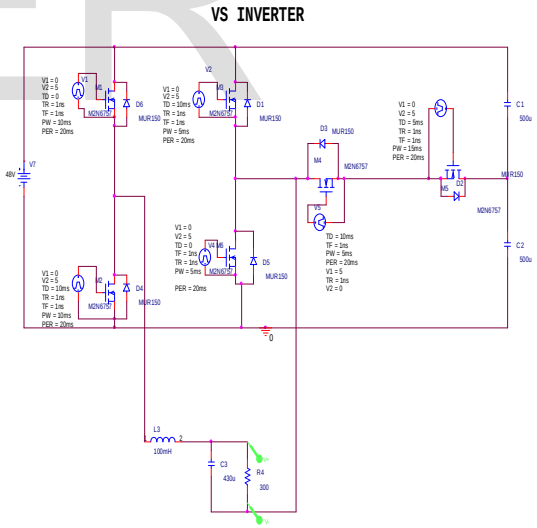

Fig.6.Simulation circuit of the proposed method

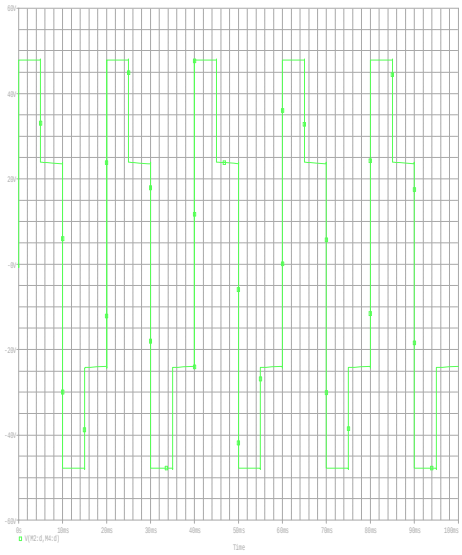

Fig.7. Output Voltage Waveform

In this proposed method, the dead time effect has been dramatically minimized , reduced the output distortion and desired rms value has been achieved.

VI CONCLUSION

In the present work, a novel method was proposed to eliminate dead time for single phase four level voltage source inverters. Compared to the conventional PWM control with dead-time, this methodreduces the output distortion and regains the rms value. It can be extended to three phase voltage source inverters. The circuits have been simulated in PSPICE and accurate results have been obtained.

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